Claim Rejections - 35 U.S.C. § 102

The Examiner has previously rejected claims 1-2, 7-8 and 12 under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

In response, applicant respectfully disagrees within the Examiner's reading of applicant's admitted prior art insofar as the Examiner within the paragraph bridging pages 2-3 of the office action mailed on 24 September 2002 characterizes applicant's thermal oxidizing process step 24 in applicant's Fig. 5 as a supplemental thermal annealing process step in accord with applicant's claim 1, clause 3 and applicant's claim 8, clause 3.

Rather, applicant's thermal oxidizing process step 24 in applicant's Fig. 5 is employed for forming applicant's third gate oxide layer 22 upon applicant's active region 11c of applicant's three times thermally oxidized semiconductor substrate 10"' (page 19, second full paragraph), and is thus not a supplemental thermal annealing process step but rather a non-supplemental thermal oxidizing process step which is employed for forming a specific gate dielectric layer of a specific thickness upon a specific active region of applicant's semiconductor substrate Within applicant's admitted prior art as illustrated in Fig. 1 to Fig. 5 and as cited by the Examiner, applicant's thermal oxidizing process steps 16, 20 and 24 are employed for forming applicant's corresponding gate dielectric layers 14a, 18a and 22 upon applicant's corresponding active regions 11a, 11b and 11c of applicant's three times thermally oxidized semiconductor substrate 10"', and thus there is no supplemental thermal annealing process step employed within applicant's admitted prior art.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art, in particular with respect to a supplemental thermal annealing process step for thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps, applicant asserts that claim 1 and claim 8 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

Since all remaining claims within this rejection are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

Claim Rejections -- 35 U.S.C. 103

The Examiner has previously rejected claims 3-6 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art.

While not precluding the existence of independent patentable distinctions between: (1) applicant's admitted prior art; and (2) that which is claimed within claims 3-6 and 9-11, applicant predicates patentability of applicant's claims 3-6 and 9-11 upon their dependence upon applicant's claim 1 or claim 8.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of applicant's claims 3-6 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art be withdrawn.

Response to Arguments

At page 3, Response to Arguments, of the office action made FINAL, applicant notes that the Examiner apparently does not in a first instance challenge applicant's assertion that the thermal oxidation process step 24 within applicant's Fig. 5 is not a supplemental thermal annealing process step in accord with applicant's claim 1, clause 3 and claim 8, clause 3 (i.e., applicant defines a supplemental thermal annealing process step as a thermal annealing process step intended to compensate for forming upon a semiconductor substrate a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps, but applicant's admitted prior art discloses a semiconductor substrate having formed thereupon a plurality (3) of gate dielectric layers having a maximum numbered plurality (3) of differing thicknesses formed employing a corresponding maximum numbered plurality (3) of thermal oxidation process steps). Thus, the Examiner apparently implicitly acknowledges that each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art.

At page 3, Response to Arguments, of the office action made FINAL, the Examiner nonetheless asserts that applicant's thermal oxidation process step 24 would be a supplemental oxidation process to gate dielectric layers already formed while at the same time being a thermal oxidation process to create gate dielectric layer 22. While the Examiner's

assertion is arguably accurate, applicant nonetheless continues to assert (and as above the Examiner apparently implicitly acknowledges) that each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art.

At page 3, Response to Arguments, of the office action made FINAL, applicant also notes that the Examiner accurately cites *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985) (see MPEP 2145) as holding that "[t]he fact than [an applicant] has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences [between the applicant's invention and the prior art] would otherwise be obvious." Thus, applicant understands that the Examiner is apparently employing the legal precedent of *Ex parte Obiaya* for purposes of supporting the Examiner's rejections of applicant's claims to applicant's invention under both 35 U.S.C. § 102 and 35 U.S.C. § 103.

In response in a first instance, applicant is not aware that legal precedent may properly be employed as a basis for rejecting an applicant's claims to the applicant's invention under 35 U.S.C. § 102. Rather, applicant understands than an applicant's claims to the applicant's invention may be properly rejected under 35 U.S.C. § 102 only when each and every limitation of the applicant's claims is disclosed within a single prior art reference. MPEP 2131. As noted above, the Examiner apparently implicitly acknowledges that each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art. Thus, applicant asserts that applicant's claim 1 and claim 8 (and claims dependent thereupon) may not properly be rejected under 35 U.S.C. § 102 as being anticipated by applicant's admitted prior art.

In response in a second instance, applicant acknowledges that an Examiner may properly employ legal precedent for purposes of providing a suggestion or motivation for modification or combination of a reference for purposes of rejecting an applicant's claims to the applicant's invention under 35 U.S.C. § 103. However, under such circumstances similarity of facts within the cited legal precedent and the applicant's application must be demonstrated. MPEP 2144, 2144.04.

As to factual similarity between *Ex parte Obiaya* and applicant's claimed invention, applicant notes that within *Ex parte Obiaya*, the pertinent prior art reference taught combustion analyzers which used labyrinth heaters to maintain combustion samples at uniform temperatures. Within *Ex parte Obiaya*, applicant appellant apparently demonstrated that a shorter response time was also obtained when employing labyrinth heaters, and it is this advantage discovered by applicant appellant which the Board felt would naturally follow from the suggestion of the prior art and was thus unpatentable. See MPEP 2145.

Within applicant's invention, applicant's admitted prior art discloses a three step thermal oxidizing method for forming three gate dielectric layers of three differing thickness upon a semiconductor substrate. Applicant's invention is not directed towards a recognition of an additional advantage which would naturally follow from applicant's admitted prior art. Rather, applicant's invention provides for a methodologic revision to the three step thermal oxidizing method for forming the three gate dielectric layers of three differing thicknesses upon a semiconductor substrate in accord with applicant's admitted prior art when it is instead desired to form three gate dielectric layers of less than three different thicknesses formed employing less than three thermal oxidizing process steps, but still maintain consistent semiconductor device performance with respect to the three semiconductor devices formed employing the three gate

dielectric layers having the less than three different thickness formed employing the less than three thermal oxidizing process steps.

In light of the above comparison, applicant does not believe that *Ex parte Obiaya* and applicant's invention are sufficiently factually similar such that the holding of *Ex parte Obiaya* may properly be employed as basis for rejecting applicant's claims to applicant's invention under 35 U.S.C. § 103, even if applicant's claims were otherwise properly rejected under 35 U.S.C. § 102.

In light of the foregoing responses, applicant continues to assert patentability of applicant's claims 1-12 over applicant's admitted prior art under both 35 U.S.C. § 102 and 35 U.S.C. § 103.

Response to Advisory Action

Within the advisory action mailed on 3 February 2003, the Examiner indicates that the thermal oxidation process step 24 within applicant's Fig. 5 can be considered a supplemental thermal annealing step since there are previous oxidations which can be considered thermal annealing steps. The Examiner also indicates that applicant's claims need to be narrowed to define over the prior art.

In response, applicant has newly added claims 13-19 which are styled after claims 1-7, but wherein applicant's supplemental thermal annealing forms no additional gate dielectric layer upon applicant's semiconductor substrate. Support for newly added claims 13-19 is found within applicant's specification at page 23, first full paragraph. In comparison, the thermal oxidation process step 24 which the Examiner asserts as a supplemental thermal annealing

process step within applicant's Fig. 5 forms a gate dielectric layer 22 upon applicant's three times thermally oxidized semiconductor substrate 10'''.

In light of the above, applicant asserts that applicant has clearly distinguished within applicant's newly added claims 13-19 applicant's invention over that which is disclosed as prior art within applicant's specification.

Other Considerations

Applicant again acknowledges the prior art of record cited by the Examiner, but not employed in rejecting applicant's claims to applicant's invention, including: (1) Su et al. (U.S. Patent No. 5,576,573); (2) Gardner et al. (U.S. Patent No. 6,054,374); (3) Jenq (U.S. Patent No. 6,303,521); (4) Pearce et al. (U.S. Patent No. 6,358,865); and (5) Mukhopadhyay et al. (U.S. Patent No. 6,399,488), as generally pertinent to applicant's invention.

No fee is due as a result of this response.

SUMMARY

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed towards a method for fabricating a semiconductor substrate to form thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps. The method employs a supplemental thermal annealing process step, which is absent from applicant's admitted prior art, to compensate for the

less than corresponding maximum numbered plurality of thermal oxidation process steps. In accord with newly added claim 13, the supplemental thermal annealing process step does not form a gate dielectric layer upon applicant's semiconductor substrate.

CONCLUSION

On the basis of the above remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

2. The method of claim 1 wherein the maximum numbered plurality is at least three.

3. The method of claim 1 wherein the maximum numbered plurality is greater than three.

4. The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

5. The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

13. (newly added) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer thereupon to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

14. (newly added) The method of claim 1 wherein the maximum numbered plurality is at least three.

15. (newly added) The method of claim 1 wherein the maximum numbered plurality is greater than three.

16. (newly added) The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

17. (newly added) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

18. (newly added) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

19. (newly added) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.